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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,903	10/29/2003	Hideki Okumura	244619US2S CIP	4526
22850	7590	08/04/2006	EXAMINER	
C. IRVIN MCCLELLAND OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			ERDEM, FAZLI	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 08/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/694,903

Applicant(s)

OKUMURA ET AL.

Examiner

Fazli Erdem

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 132). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

NATHAN J. PLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

- 1) ☒ Responsive to communication(s) filed on 28 June 2006.
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6, 8, 9, 12-17, 21-26 and 28-35 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☒ Claim(s) 8, 12-15, 21-25, 31, 33 and 35 is/are allowed.
6) ☒ Claim(s) 1-6, 9, 16, 17, 26 and 28-30 is/are rejected.
7) ☒ Claim(s) 32-34 is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____

DETAILED ACTION

Per Examiner interview on 06/9/2006, the final action issued on 03/16/2006 has been withdrawn and after further search/consideration this non-final action has been issued.

Allowable Subject Matter

1. Claims 8, 12-15, 21-25, 31, 33 and 35 allowed.
2. Claim 32 and 34 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-3, 5, 9, 16, 17 and 28-30 rejected under 35 U.S.C. 103(a) as being unpatentable over Leung et al. (6,653,718) in view of Brewer et al. (6,322,600).

Regarding Claims 1-3, 5, 9, 16, 17 and 28-30, Leung et al. disclose a semiconductor device where in Fig. 4, substrate 45, column 8, line 52, with a trench 42, column 8 line 52, a particulate insulating layer 46/47, column 8 line 56, filling at least a lower portion of trench and comprising insulating silica particles and a reflowable infiltrating matrix material dielectric layer, column 8 line 57 covering an upper surface of the particulate insulating layer 46/47. Reflowable dielectric layer of infiltrating matrix

material 48 comprises silicate glass doped with impurity as shown in column 6, line 12 and claim 15. Barrier insulating layer 44 as shown in column 8 line 52, on a sidewall and a bottom surface of the trench, as shown in Fig. 4 where the particulate insulating layer further comprises an insulating binder, column 4 line 60. Furthermore, in column 4 line 29, diameter of the insulating particle falls within the required range. Finally, barrier insulating layer 44 on a sidewall and a bottom surface of the trench where the first and second insulating particles are mixed as in Fig. 4. Although, the prior art does not specially disclosed the claimed limitation “the insulating particles being stable at melting point or a softening point of the reflowable dielectric layer”, this feature is seen to be inherent teaching of that limitations because the silica particle has the melting point of more than 1500 Celcius while the dielectric PSG or BPSG is typically around 800 Celcius. Leung et al. fail to disclose the required diameter size for the insulating particles. However, Brewer et al. disclose planarization compositions where in the abstract section the required diameter size for the insulating particles are disclosed.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required insulating particles size in Leung et al. as taught by Brewer et al. in order to have a semiconductor device with bettering insulation characteristics.

Regarding Claim 2, Leung discloses a device where the reflowable dielectric layer 48 comprises silicate glass doped with impurity, column 6, line 12 and claim 15

Regarding Claims 3,5, 17 and 28-30 Leung discloses a device further comprising a barrier insulating layer 44, column 8 line 52 on a sidewall and a bottom surface of trench Fig. 4, where the particulate insulating layer further comprises an insulating binder, column 4 line 60.

Regarding Claims 1, Leung discloses the device where the average diameter of the insulating particle falls within a range of 100 nm to 500 nm as shown in column 4 line 29.

Regarding Claim 8, Leung discloses semiconductor device in Fig. 4, comprising substrate with a trench 42 and a particulate insulating layer 46/47 filling at least a lower portion of the trench 42 and comprising first and second insulating particles, an average diameter size of the second insulating particles being smaller than average diameter of first insulating particles as shown in column 4, line 45-49.

Regarding Claim 9, in Fig. 4 first and second insulating particles are mixed.

Regarding Claims 16, Leung discloses a semiconductor substrate 45 with a trench 42 and particulate insulating layer 46/47 filling at least a lower portion of the trench and comprising insulating particles and an insulating binder in column 4 line 60, that bonds the insulating particles together, the insulating particles and the insulating binder forming a network structure where the average diameter of the insulating material falls within a range of 100 nm to 500 nm

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

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having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 4, 6, and 26 rejected under 35 U.S.C. 103(a) as being unpatentable over Leung et al. (6,653,718) in view of Brewer et al. (6,322,600) further in view of Gu et al. (6,551,901).

Regarding Claims 4, 6, and 26 Leung et al. disclose a semiconductor device where in Fig. 4, substrate 45, column 8, line 52, with a trench 42, column 8 line 52, a particulate insulating layer 46/47, column 8 line 56, filling at least a lower portion of trench and comprising insulating silica particles and a reflowable infiltrating matrix material dielectric layer, column 8 line 57 covering an upper surface of the particulate insulating layer 46/47. Reflowable dielectric layer of infiltrating matrix material 48 comprises silicate glass doped with impurity as shown in column 6, line 12 and claim 15. Barrier insulating layer 44 as shown in column 8 line 52, on a sidewall and a bottom surface of the trench, as shown in Fig. 4 where the particulate insulating layer further comprises an insulating binder, column 4 line 60. Furthermore, in column 4 line 29, diameter of the insulating particle falls within the required range. Finally, barrier insulating layer 44 on a sidewall and a bottom surface of the trench where the first and second insulating particles are mixed as in Fig. 4. Leung does not disclose the device with the required insulating particles with the required average diameter further comprising a cap insulating layer covering an upper surface of the reflowable dielectric layer. However, Brewer et al disclose planarization compositions where in the abstract section the required dielectric particles with the required average diameter size are disclosed. Furthermore, Gu et al. disclose a shallow trench isolation in Fig 14,

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comprising a cap insulating layer 1408 and in column 5 line 31, covering an upper surface of the reflowable dielectric layer 1304 in column 5 line 11.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required cap insulating layer in Leung et al. as taught by Gu et al. in order to have a semiconductor device with better reliability.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fazli Erdem whose telephone number is (571) 272-1914. The examiner can normally be reached on M - F 8:00 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

FE
August 1, 2006

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